



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA



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Customizable Die-to-Die Interconnect for AI Chipllets

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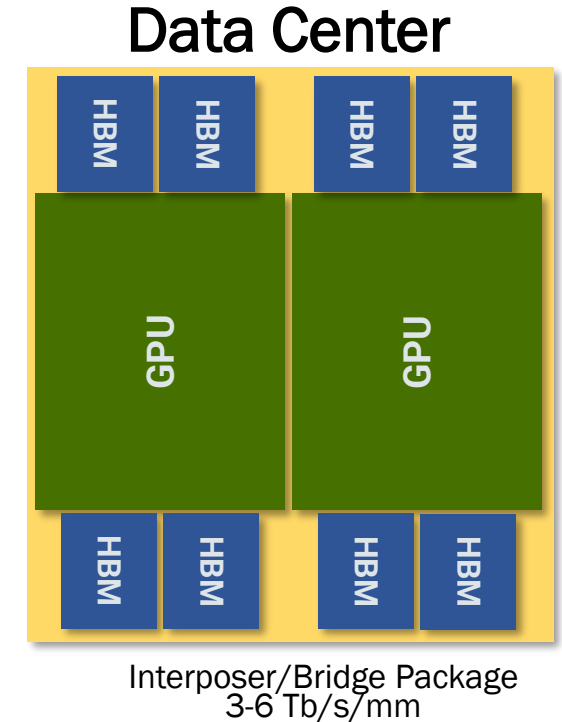
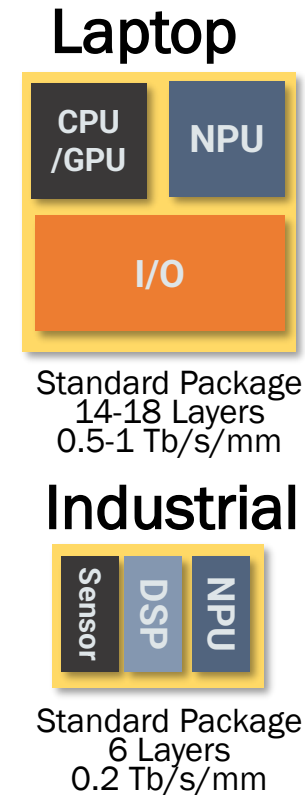
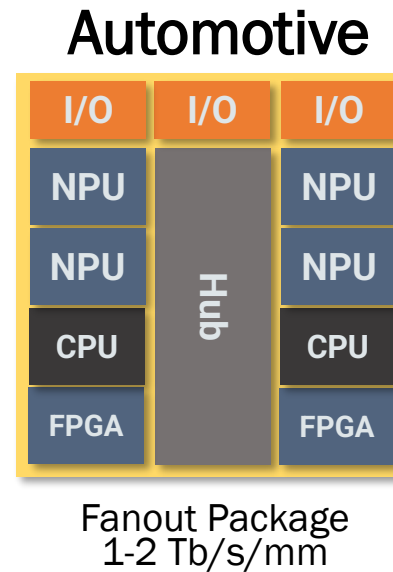
The Rise of Chiplets

- Chiplets have emerged as a key implementation paradigm due to their cost benefits
- Manufacturing cost optimization is the most well-proven and clear benefit of chiplets
 - Chiplets allow for yield and process technology optimization – even when used to stitch together reticle sized dies



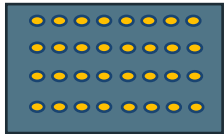
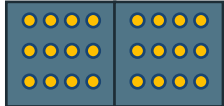
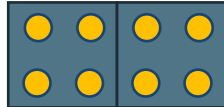

AI Is Everywhere

- And hence chiplets are too
- Requirements placed on the die-to-die (D2D) interconnect vary widely with the application / product
 - Package type, bandwidth, power, reach, footprint, protocols, ...



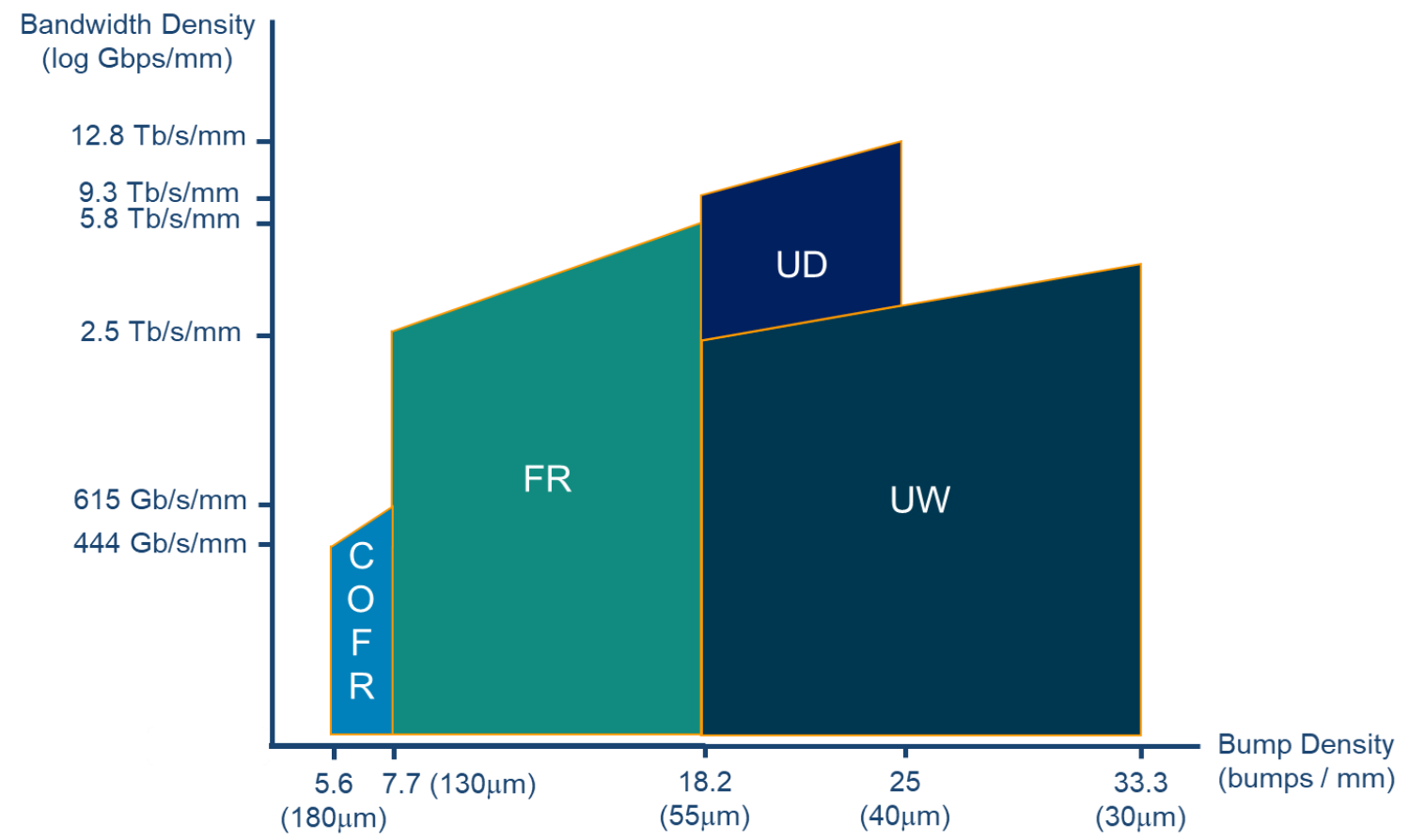
No One Size Fits All

- But D2D PHYs can be categorized by package type, bandwidth, reach, and hence energy-efficiency

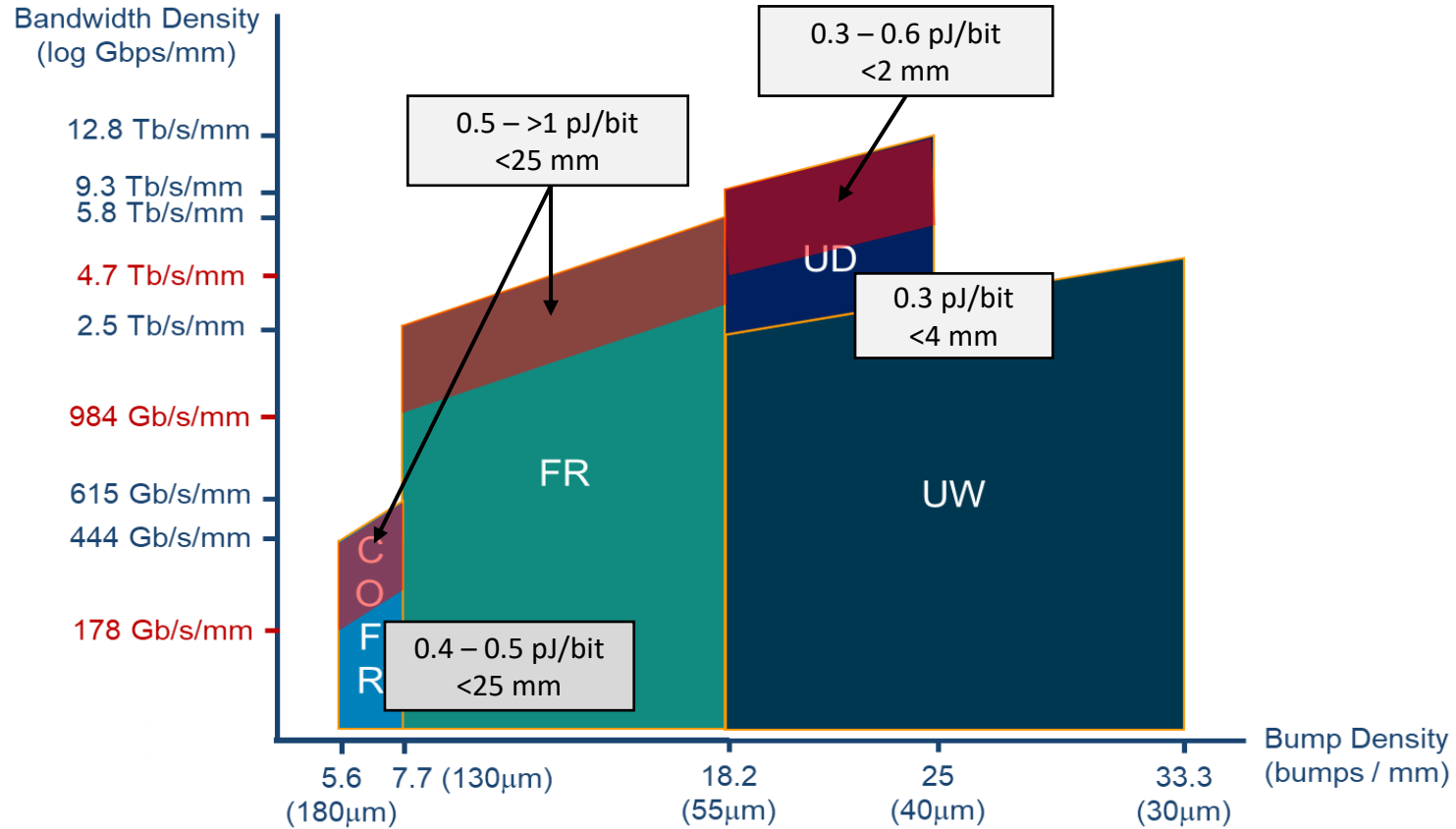
Category	Package	Per-Line Rate	Reach	Energy/Bit	
Ultra Wide (UW)	Advanced only ($<55\text{ }\mu\text{m}$ pitch)	$< 8\text{ Gb/s}$	$<4\text{mm}$	$\sim 0.3\text{ pJ}$	
Ultra Dense (UD)	Advanced only ($40\text{-}55\text{ }\mu\text{m}$ pitch)	$8 - 32\text{ Gb/s}$	$<2\text{mm}$	$\sim 0.3 - 0.6\text{ pJ}$	
Full Reach (FR)	Standard or fanout ($55\text{-}130\text{ }\mu\text{m}$ pitch)	$< 40\text{ Gb/s}$	$<25\text{mm}$	$\sim 0.4 - >1\text{ pJ}$	
Cost-Optimized Full Reach (CO-FR)	Low-layer standard ($130\text{-}180\text{ }\mu\text{m}$ pitch)	$< 40\text{ Gb/s}$	$<25\text{mm}$	$\sim 0.4 - >1\text{ pJ}$	

Die Edge

Bandwidth Density vs. Bump Density



Bandwidth Density vs. Bump Density

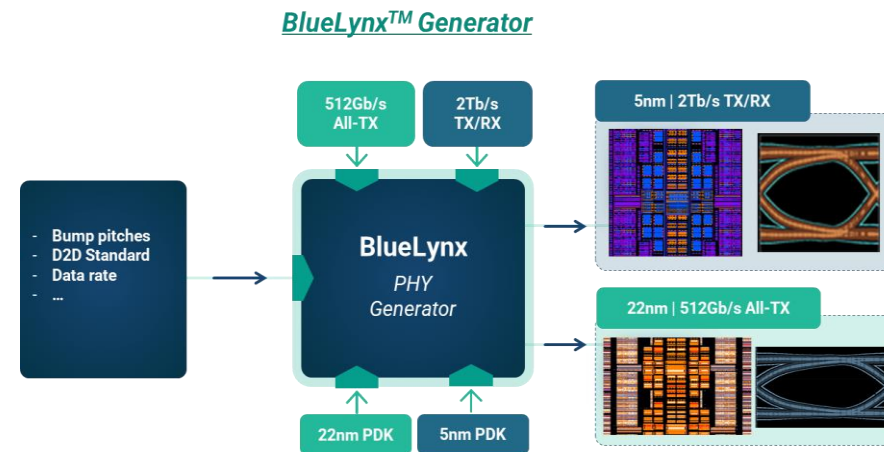


Applications

Category	Typical Applications
Ultra Wide (UW)	FPGAs
Ultra Dense (UD)	Custom AI silicon, HPC
Full Reach (FR)	Data center, edge, infrastructure, automotive
Cost-Optimized Full Reach (CO-FR)	Consumer, industrial

Blue Cheetah Delivers Customized D2D Interfaces

- We internally leverage our generator based automation to rapidly deliver customized D2D interface solutions to our customers



- BCA architecture + generator spans the full CO-FR, FR, UW, and UW design space
 - Broad variety of chiplets (AI accelerators, CPUs, I/O hubs, memory, and more) being built on *BlueLynx™* interconnects today

Conclusions

- Chiplets are emerging as a key implementation strategy for the full spectrum of AI hardware / silicon
 - Cost optimization and time-to-market are the key considerations leading to chiplets
- AI is everywhere, and there are no one size silicon (chiplet) solutions
 - The D2D interconnect for these chiplets must be tailored along with their end applications
- Blue Cheetah works closely with our partners and customers to ensure the D2D interconnect is the perfect fit for their chiplet products